

What is claimed is:

1. An execution architecture, the architecture comprising:
 - a memory array, the array having first and second blocks, first and second I/O ports, first and second address ports, and a configuration control port, where a first value of a configuration control signal received at the configuration control port configures the first block to be coupled to the first I/O port and the first address port and the second block to be coupled to the second I/O port and the second address port, and a second value of the configuration control signal configures the first block to be coupled to the second I/O port and the second address port and the second block to be coupled to the first I/O port and the first address port;
 - a data controller and address generator (DCAG) having an address output port and a control input port, the address output port of the DCAG being coupled to the first address port of the memory array and the DCAG being configured to generate address values at the DCAG address output port responsive to a vector data control signal received at the DCAG control input port;
 - a DMA controller and address generator (DMACAG) having an address output port and a control input port, the address output port of the DMACAG being coupled to the second address port of the memory array and the DMACAG being configured to generate address values at the DMACAG address output port responsive to a DMA control signal received at the DMACAG control input port;
 - a first execution unit having first and second I/O ports, the first I/O port of the first execution unit being coupled to the first I/O port of the memory array;
 - a first local memory array having a first I/O port and a first address port, the first I/O port of the first local memory being coupled to the second I/O port of the first execution unit; and
 - a first local address generator (LAG) having an address output port and a control input port, the address output port of the first LAG being coupled to the first

address port of the first local memory array and the first LAG being configured to generate address values at the first LAG address output port responsive to a first execution control signal received at the first LAG control input port.

5 2. The execution architecture of claim 1, including a memory centric controller (MCC) configured to generate the configuration control signal, the vector data control signal, the DMA control signal and the first execution control signal, where the MCC is configured to switch the first and second blocks of the memory array and drive the DCAG and DMACAG independently of one another to
10 simultaneously transfer data through the first and second I/O ports of the memory array and the MCC is configured to independently drive the first LAG to transfer data between the first local memory and the first execution unit.

 3. The execution architecture of claim 2, wherein the configuration
15 control signal, the vector data control signal, the DMA control signal and the first execution control signal are each microcode values generated by the MCC.

 4. The execution architecture of claim 1, including a sequencer configured to generate the configuration control signal, the vector data control signal,
20 the DMA control signal and the first execution control signal, where the sequencer receives a status signal from each of the first EU, first LAG, DCAG, and DMACAG and generates values for the configuration control signal, the vector data control signal, the DMA control signal and the first execution control signal responsive to the status signal from each of the first EU, first LAG, DCAG, and DMACAG and a
25 microcode program.

5. The execution architecture of claim 4, wherein the values for the configuration control signal, the vector data control signal, the DMA control signal and the first execution control signal are microcode control words.

5 6. The execution architecture of claim 1, the architecture including:
an execution unit interface unit interposed the execution unit and the memory array and having a first I/O port coupled to the first I/O port of the execution unit and a second I/O port coupled to the first I/O port of the memory array, a control input port configured to receive an execution unit interface control signal, and a first wide
10 buffer, where a first predetermined number of words of the first wide buffer is proportional to a ratio of an execution speed of the execution unit to an access speed of the memory array and the execution unit interface unit transfers individual words of data between the execution unit and the first wide buffer and transfers the first predetermined number of words between the first wide buffer and the memory array
15 responsive to the execution unit interface control signal.

7. The execution architecture of claim 1, the architecture including:
a bus interface unit coupled between the second port of the memory array and a system bus, where the bus interface unit having a first I/O port coupled to the second
20 I/O port of the memory array and a second I/O port coupled to the system bus, a control input port configured to receive a bus interface control signal, and a second wide buffer, where a second predetermined number of words of the second wide buffer is proportional to a ratio of a transfer speed of the system bus to an access speed of the memory array and the bus interface unit transfers individual words of
25 data between the system bus and the second wide buffer and transfers the second predetermined number of words between the second wide buffer and the memory array responsive to the bus interface control signal.

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8. The execution architecture of claim 1, including:

a second local address generator (LAG) having an address output port and a control input port, and the second LAG being configured to generate address values at the second LAG address output port responsive to a second execution control signal
5 received at the second LAG control input port; and

wherein the first local memory includes first and second blocks, a second I/O port, a second address port and a configuration control input, where, responsive to a first value of a local memory configuration control signal received at the configuration control input, the first block of the first local memory is coupled to the
10 first I/O port and first address port and the second block of the first local memory is coupled to the second I/O port and second address port and where, responsive to a second value of the local memory configuration control signal, the first block of the first local memory is coupled to the second I/O port and second address port and the second block of the first local memory is coupled to the first I/O port and first address
15 port, the address output port of the second LAG being coupled to the second address port of the first local memory.

9. The execution architecture of claim 8, wherein the second I/O port of the first local memory is coupled to a microcode store.

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10. The execution architecture of claim 1, wherein the memory array includes a third block coupled to a third I/O port and a third address port of the memory array, wherein the third block of the memory array is configured to be switched with the first and second blocks of the memory array responsive to the
25 configuration control signal and including:

another data controller and address generator (DCAC) having an address output port and a control input port, the address output port of the another DCAG being

coupled to the third address port of the memory array and the DCAG being configured to generate address values at the DCAG address output port responsive to another vector data control signal received at the second DCAG control input port;

5 a second execution unit having first and second I/O ports, the first I/O port of the first execution unit being coupled to the third I/O port of the memory array;

a second local memory array having an I/O port and an address port, the I/O port of the second local memory being coupled to the second I/O port of the second execution unit; and

10 a second local address generator (LAG) having an address output port and a control input port, the address output port of the second LAG being coupled to the address port of the second local memory array and the second LAG being configured to generate address values at the second LAG address output port responsive to a second execution control signal received at the second LAG control input port.

15 11. The execution architecture of claim 10, wherein:
the first local memory includes a codec microcode program; and
the second local memory includes a motion estimation microcode program.

20 12. The execution architecture of claim 11, wherein the architecture is configured to operate as an MPEG-2 encoder.

13. The execution architecture of claim 1, wherein the first execution unit includes:

25 a combination multiplier/arithmetic logic unit (ALU) block having first and second input ports and an output port; and

a vector register file having a first I/O port coupled to the first I/O port of the first local memory, a second I/O port coupled to the first I/O port of the memory

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array, a first output port coupled to the first input port of the combination multiplier/ALU block, a second output port coupled to the second input port of the combination multiplier/ALU block, and a first input port coupled to the output port of the combination multiplier/ALU block, where the vector register file includes
5 multiple register blocks configured to be independently coupled to the first and second I/O ports, the first and second output ports and the input port of the vector register file responsive to a vector register control signal, where a word size of each of the multiple blocks is independently configurable by the vector register control signal to match a transfer rate of each of the ports of the vector register file.

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